REMARKS/ARGUMENTS

Claims 1-21 stand rejected in the outstanding Official Action. Claims 1, 5, 9, 11, 15, 19 and 21 have been amended and therefore claims 1-21 remain in this application.

The abstract of the disclosure is objected to because it exceeds 150 words. Applicant has offered a substitute abstract with less than 150 words, thereby obviating the objection.

The Examiner has required formal drawings in this application and Applicant encloses two substitute sheets of drawings in formal form. Entry of the formal drawings is believed to obviate the drawing requirement.

The drawings are objected to under Rule 83 as allegedly failing to show every feature of the invention specified. The Examiner contends that the drawings fail to show "the additional pipeline stages" as disclosed in claims 5, 9, 15 and 19. The Examiner's attention is directed to Figure 1 in which offset register 82 comprises the "additional pipeline stage." This is specifically disclosed in Applicant's specification, page 15, lines 3-7. As a result, Applicant's originally submitted drawings, as well as the attached substitute drawings, clearly identify an additional pipeline stage in the form of "offset register 82." Thus, the "additional pipeline stages" as recited in claims 5, 9, 15 and 19 are clearly shown in the originally filed drawings as well as the substitute drawings and any further objection thereto is respectfully traversed.

The Examiner also suggests that the "address generation paths" disclosed in claims 1-21 are not disclosed in the drawings. As described in Applicant's specification, page 14, line 29 to page 15, line 2, the address generation paths are a series of elements rather than an individually numbered structure. As stated in the specification, page 14, lines 29-31, "a first address generation path can be seen to be provided by multiplexer 85, address adder 90 and multiplexer

46" which path is used to generate a target address for the first prefetched instruction. A second (and further) address generation path is formed by the offset multiplexer 80, offset register 82, multiplexer 85, address adder 90 and multiplexer 46 to provide the target address for any other prefetched instructions. Thus, the elements creating the "first" and "at least one further" address generation paths are clearly disclosed in Applicant's drawings and described in Applicant's specification. As a result, the requirements of Rule 83 have been clearly met and any further objection thereto is respectfully traversed.

Claims 5, 9, 15 and 19 stand rejected under 35 USC §112 (first paragraph) as failing to comply with the enablement requirement. As the Examiner has indicated on page 4 of the Official Action, "the only way that adding a pipeline stage can increase generation speed is by adding a pipeline stage to break up a critical path." What the Examiner apparently did not appreciate was that the "offset register 82" disclosed in Figure 1 comprises the "additional pipeline stage" and therefore this is clearly shown in the drawings and described in Applicant's specification, as noted above.

The Examiner apparently appreciates that in a clocked system, the clock frequency has to be set with respect to the slowest path. However, to enable a speed benefit of the first address generation path to be realized, the pipeline stage in the form of offset register 82 is provided in the at least one further address generation path. Those of ordinary skill in the art will appreciate that this increases the number of clock cycles taken in at the at least one further generation path. This enables the potential speed benefits of the simplified first address generation path to be realized, since the clock speed is now not limited by the complex "at least one further address generation path." As a result, provision of the offset register 82 in the "at least one further

address generation path" increases the speed of generation of the target address by the first address generation path because it allows a higher clock speed to be used in both address generation paths.

As the Examiner appreciates, considering the particular embodiment shown in Figure 1, a multi-input multiplexer is slower in operation than a single input multiplexer. As a result, the application of the first address generation path from holding register 95 applied as an input to decode block 78 and providing the output directly to multiplexer 85 and the remainder of the address generation path (address adder 90 and multiplexer 46) operates significantly faster than the further address generation paths going through decoders 72, 74, 76 through multiplexer 80 and offset register 82 as well as the additional address generation path elements (address adder 90 and multiplexer 46).

In view of the above discussion and the identification of those elements comprising the first and further address generation paths contained in the originally filed drawings and discussed in Applicant's specification in the paragraphs bridging pages 14 and 15, it is submitted that claims 5, 9, 15 and 19 are clearly supported and there is no basis for rejection under 35 USC §112 and any further rejection thereunder is respectfully traversed.

The Examiner alleges that should claim 1 be found allowable, claim 21 will be objected to as being a substantial duplicate. Applicant's claim 1 is directed to a "data processing apparatus" which includes a particularly specified element, i.e., a "prefetch unit." Applicant's claim 21 is limited to only the "prefetch unit" thereby covering only a subset of claim 1, but claiming that subset in independent form. Applicant is entitled to have independent claims of varying scope. Rule 75 does not prevent the existence of more than one independent claim, even

though portions of the claim wording is similar or identical between the two claims as long as the two claims are directed to substantially different subject matter. Claim 1 is directed to "a data processing apparatus" and claim 21 is directed to "a prefetch unit." The different scope of these claims is believed more than sufficient to warrant patentability of each of these independent claims and therefore any further contention that these claims are substantial duplicates of one another is respectfully traversed.

Claims 1-4, 6-8, 10-14, 16-18 and 20 stand rejected under 35 USC §102 as allegedly being anticipated by Furber ("ARM System-on-Chip Architecture"). The Court of Appeals for the Federal Circuit has noted in the case of *Lindemann Maschinenfabrik GMBH v. American Hoist & Derrick*, 221 USPQ 481, 485 (Fed. Cir. 1984) that "[a]nticipation requires the presence in a single prior art reference disclosure of each and every element of the claimed invention, arranged as in the claim."

Independent claims 1, 11 and 21 both originally required address generation logic "having a first address generation path" and "at least one further address generation path." Additionally, a portion of claim 5 relating to the provided "pipeline stage" has been added to independent claims 1, 11 and 21. None of the above three limitations are believed to be disclosed in the Furber reference.

While the Examiner generally cites page 388 of Furber as containing a disclosure of the address generation logic, i.e., the "first address generation path" and the "at least further address generation path," there is believed to be no disclosure of these address generation paths in the Furber reference. Should the Examiner believe otherwise, he is requested to indicate the location of such disclosure. In fact, Furber discloses a branch prediction unit, split into two 8-entry

halves, with branches at even half-word addresses stored in one half and branches at add half-word addresses stored in the other half (see page 388). Even assuming these are Applicant's claimed two address generation paths, this contradicts the claim which has the first prefetched instruction handled in the first address generation path and all others being handled in the at least one further address generation path.

While the Examiner argues that Furber has a first address generation path which generates a target address "more quickly" than the other address path, this contention is respectfully traversed. It is to be noted that Furber merely discloses that if branch instructions "hit" in both halves of its branch prediction unit, then the "even address" takes priority. This does not suggest that one path generates an address more quickly than the other, but merely decides to produce a target address preferentially from one path over the other. There is nothing suggesting that the selection happens any faster for one path than the other, and indeed there is no structure or interrelationship which would suggest any difference in speed.

Also, as noted above, claims 1, 11 and 21 have been amended to reference the provision of a pipeline stage in the at least one further address generation stage. There appears to be no such distinction in the Furber reference and, indeed, in the rejection under §102, the Examiner does not contend that this aspect of claim 5 (now added to the independent claims) is disclosed in Furber.

In view of the above, there is simply no support for a rejection of claims 1-4, 6-8, 10-14, 16-18 and 20 under 35 USC §102 as anticipated by Furber and therefore any further rejection thereunder is respectfully traversed.

On page 12 of the Official Action, the Examiner discusses claim 21, but there is no indication contained in the Official Action as to whether claim 21 is being rejected or under which portion of the statute. If the Examiner contends that claim 21 is either anticipated or obvious in view of Furber, it is noted that claim 21 also includes the previously discussed address generation paths as well as being recently amended to include the recited "pipeline stage." Thus, the above comments with respect to claim 1 distinguishing claim 21 over the Furber reference are herein incorporated by reference.

Claims 7, 8, 17 and 18 stand rejected under 35 USC §103 as unpatentable over Furber in view of Hara (U.S. patent 5,848,269). Inasmuch as claims 7, 8, 17 and 18 ultimately depend from claims 1 and 11, the above distinctions of claims 1 and 11 over the Furber reference are herein incorporated by reference. There is no disclosure or suggestion by the Examiner that Hara teaches the missing "address generation paths" or "pipeline stage" required by claims 1, 11 and 21. Consequently, claims 7, 8, 17 and 18 cannot be obvious in view of the Furber/Hara combination and any further rejection thereunder is respectfully traversed. Moreover, the Examiner has failed to provide any reason or motivation for combining the Furber and Hara references and therefore has failed to establish a *prima facie* basis of obviousness.

Claims 5 and 15 stand rejected under 35 USC §103 as unpatentable over Furber in view of Patterson. Again, claims 5 and 15 depend from claims 1 and 11 and therefore the above comments distinguishing claims 1 and 11 from the Furber reference are herein incorporated by reference. Applicant notes that the Examiner does not contend that the address generation paths and pipeline stage missing from Furber are disclosed in Patterson. Accordingly, even if Furber and Patterson could be combined, they do not disclose the subject matter of Applicant's

independent claims 1 and 11 and thus cannot disclose the subject matter of dependent claims 5 and 15. Moreover, there is simply no reason or suggestion for combining the Furber and Patterson references and therefore there is no *prima facie* basis of obviousness in view thereof.

Claims 5 and 15 are also rejected under 35 USC §103 as unpatentable over Furber/Hara/Patterson combination and the above comments with respect to claims 1 and 11, from which claims 5 and 15 depend, are herein incorporation by reference, both with respect to the Furber/Hara combination as well as the Furber/Hara/Patterson combination and the Furber/Patterson combination.

Having responded to all objections and rejections set forth in the outstanding Official Action, it is submitted that pending claims 1-21 are in condition for allowance and notice to that effect is respectfully solicited. In the event the Examiner is of the opinion that a brief telephone or personal interview will facilitate allowance of one or more of the above claims, he is respectfully requested to contact Applicant's undersigned representative.

Respectfully submitted,

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AMENDMENTS TO THE DRAWINGS

Please enter the two sheets of substitute drawings attached hereto.